# PATENT ABSTRACTS OF JAPAN

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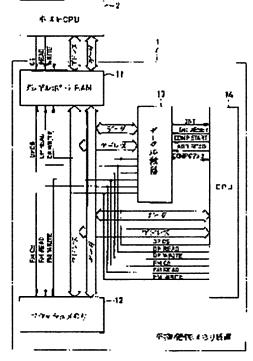
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## (54) NON-VOLATILE MEMORY DEVICE

## (57)Abstract:

PROBLEM TO BE SOLVED: To improve the reliability and at the same time, achieve a speedy access without causing the reduction in processing speed of an upper device. SOLUTION: A data comparator 13 compares data stored in a dual-port RAM 11 with data stored in a flash memory 12 successively from a start address to a final address. The data comparator 13 outputs an interrupt signal to a CPU 14 when it detects the non-coincidence of data. The CPU 14 erases the erasure block of the flash memory 12 including an address inputted from the data comparator 13 when an interrupt signal is inputted and reads data within the erasure block range from the dual-port RAM 11 and writes the data into the flash memory 12. When the non-volatile memory device 1 is turned on, the CPU 14 transfers all data of the flash memory 12 to the dual-port RAM 11.



## **LEGAL STATUS**

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#### **CLAIMS**

# [Claim(s)]

[Claim 1] The flash memory which memorizes the data from high order equipment, and the storing means which carries out a temporary storage before memorizing the data from said high order equipment to said flash memory with the same capacity as the capacity of said flash memory, A comparison means to compare the data memorized by said flash memory with the data stored in said storing means, Nonvolatile memory equipment characterized by having the means which writes the data with which it corresponds within said storing means after performing elimination processing to the field of said flash memory to which the data with which the inequality was detected are memorized, when an inequality is detected by said comparison means in said field.

[Claim 2] Nonvolatile memory equipment according to claim 1 characterized by including a means to transmit the contents of said flash memory to said storing means when a power source is switched on. [Claim 3] Said storing means is nonvolatile memory equipment according to claim 1 or 2 characterized by consisting of random access memory including two or more input/output port in which write-in readout is free.

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#### DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the nonvolatile memory equipment used for the audio file equipment which changes an analog sound signal into a PCM (Pulse Code Modulation) digital signal, and memorizes it about nonvolatile memory equipment.
[0002]

[Description of the Prior Art] Conventionally, in this kind of audio file equipment, by A/D (analog/digital) conversion, an analog sound signal is changed into a PCM digital signal, and is accumulated in record media, such as semiconductor memory and a magnetic disk.

[0003] With audio file equipment, the analog sound signal is reproduced by carrying out D/A (digital/analog) conversion of read-out and its PCM digital signal for the PCM digital signal accumulated in the record medium. Since this audio file equipment is used as record and a regenerative apparatus of the CM (commercials) and the program which are mainly used by radio television broadcasting and repetition use is carried out for a long period of time in the case of CM etc., advanced dependability is required from a record medium.

[0004] Moreover, since a sound signal is digital-signal-ized and is processed at the high speed, it has input/output port of the analog signal which can be processed to coincidence to one audio file equipment.

[0005] Although the hard disk drive unit is used as a record-medium part of above audio file equipment, since a hard disk drive unit is a machine product, it is unreliable, since MTBF (Mean Time Between Failures: prediction Mean Time Between Failure) is also about two years, a periodical overhaul is needed and a running cost increases.

[0006] Therefore, in the field as which real time access called record of voice or an image is required, semiconductor memory with high-speed DRAM (Dynamic Random Access Memory) or SRAM (Static Random Access Memory) etc. is used. Moreover, since these DRAMs and SRAM are volatile memory, even when a power source is disconnected, the treatment of a battery back-up etc. is needed for holding data.

[0007]

[Problem(s) to be Solved by the Invention] With the conventional audio file equipment mentioned above, semiconductor memory with DRAM, SRAM, etc. high-speed as a record medium is used, and even when a power source is disconnected, in order to hold data, the measures of a battery back-up etc. are taken.

[0008] However, since the dc-battery used for the treatment of a battery back-up etc. is also about two years, MTBF needs to overhaul periodically it. [ as well as a hard disk drive unit ] [0009] Although there is a flash memory as the same high-speed semiconductor memory as DRAM, SRAM, etc., the writing of data to a flash memory needs to write in data, after eliminating memory block which should write in data unlike the writing of the data in DRAM, SRAM, etc. [0010] Therefore, when a flash memory is used as a record medium, in order to have to perform

elimination actuation to a flash memory first, it must wait for the writing to memory block until the elimination actuation finishes. That is, since the write time is late compared with DRAM or SRAM although dependability improves and it becomes a maintenance free when a flash memory is used, it is difficult to use a flash memory for the audio file equipment with which it is required of real time access. [0011] There is a technique which enabled it to perform other processings in JP,62-123521,A, without not passing a bus royalty to DMA for the data of a floppy disk drive unit by having DMA and buffer memory of dedication in the data transfer of a floppy disk drive unit, and CPU (central processing unit) stopping also in a transfer.

[0012] With this technique, either the address from the memory direct access device and its memory direct access device of the dedication over control of a floppy disk drive unit or the addresses of CPU are also equipped with the local data bus connected to the data bus connected to accessible buffer memory, and this buffer memory and CPU, buffer memory and a data bus, and the control device of a floppy disk drive unit, and they make data transfer possible between a floppy disk drive unit and buffer memory through the local data bus with the memory direct access device.

[0013] When performing a data access between CPU and a floppy disk drive unit, after a floppy disk drive unit takes out BASURI QUEST to CPU, occupies a bus, stops actuation of CPU, and performing a data access between a floppy disk drive unit and main memory, releasing a bus and releasing a bus, processing in which CPU accesses main memory is performed.

[0014] In this art, since actuation of CPU cannot be performed while performing the data access, if a data access with a floppy disk drive unit occurs, the processing speed of that system will fall. [0015] In order to prevent the fall of the processing speed, it has the buffer memory to which either can also perform a data access independently between a floppy disk drive unit and CPU. Since it is not necessary by this to stop actuation of CPU also while performing the data access between a floppy disk drive unit and buffer memory, the fall of processing speed can be prevented.

[0016] However, since actuation of a central processing unit is kept waiting until the data access between buffer memory and a floppy disk drive unit serves as [ the capacity of buffer memory ] a low speed since it is small compared with the capacity of a floppy disk drive unit, and the data access is completed, processing speed will fall.

[0017] Moreover, since CPU needs to control a floppy disk drive unit to perform a data access between buffer memory and a floppy disk drive unit, this becomes the factor which causes the fall of processing speed.

[0018] Then, it is in offering the nonvolatile memory equipment which can access a high speed, without causing the fall of the processing speed in high order equipment, while the purpose of this invention can cancel the above-mentioned trouble and can improve dependability.

[Means for Solving the Problem] The flash memory the nonvolatile memory equipment by this invention remembers the data from high order equipment to be, The storing means which carries out a temporary storage before memorizing the data from said high order equipment to said flash memory with the same capacity as the capacity of said flash memory, A comparison means to compare the data memorized by said flash memory with the data stored in said storing means, When an inequality is detected by said comparison means, after performing elimination processing to the field of said flash memory to which the data with which the inequality was detected are memorized, it has the means which writes the data with which it corresponds within said storing means in said field.

[0020] The nonvolatile memory equipment by this invention is equipped with a means to transmit the contents of said flash memory to said storing means when the power source other than the abovementioned configuration is switched on.

[0021]

[Embodiment of the Invention] First, an operation of this invention is described below. [0022]

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## TECHNICAL FIELD

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## EFFECT OF THE INVENTION

[Effect of the Invention] The dual port RAM which carries out a temporary storage before memorizing the data from high order equipment to a flash memory with the capacity same according to this invention as the capacity of the flash memory which memorizes the data from high order equipment, as explained above is formed. The data with which a dual port RAM corresponds after performing elimination processing to the field of a flash memory to which the data with which the inequality was detected are memorized, when an inequality is detected by the comparison with the data memorized by the flash memory and the data stored in the dual port RAM It is effective in the ability to access a high speed, without causing the fall of the processing speed in high order equipment, while being able to improve dependability by writing in the field.

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#### TECHNICAL PROBLEM

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memory of dedication in the data transfer of a floppy disk drive unit, and CPU (central processing unit)

memory through the local data bus with the memory direct access device.

[0013] When performing a data access between CPU and a floppy disk drive unit, after a floppy disk drive unit takes out BASURI QUEST to CPU, occupies a bus, stops actuation of CPU, and performing a data access between a floppy disk drive unit and main memory, releasing a bus and releasing a bus, processing in which CPU accesses main memory is performed.

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